PACSystems* RX3i

IC695RMX128-FH

Redundancy Memory Xchange Module

GFK-2511M
March 2016

The PACSystems* Redundancy Memory Xchange (RMX) module operates as a node on a reflective memory network or as a dedicated link between CPUs in an RX3i Hot Standby CPU Redundancy system. When the RMX is not being used as a link in a redundancy system, it is functionally identical to the IC695CMX128 module. Each node in the network can be any reflective memory device that is compatible with the 5565 family. Whenever data is written to one node, all nodes on the network are automatically updated with the new data.

When used as a node on a reflective memory network, the RMX module provides deterministic sharing of data among PLCs and other computing devices on a high-speed fiber-optic network. A reflective memory network can contain up to 256 nodes.

Each node in the reflective memory network is connected in a daisy-chained loop using fiber-optic cables. The transmitter of the first node is tied to the receiver of the second. The transmitter of the second node is tied to the receiver of the third node, and so on, until the loop is completed at the receiver of the first node.

When used in a CPU redundancy system, the RMX modules provide a path for transferring data between the two redundancy CPUs in the redundant system. A complete communications path consists of one RMX in the primary unit, one RMX in the secondary unit, and two high-speed fiber-optic cables connecting them to each other. This must be a two-node ring: no other reflective memory nodes are allowed to be part of this fiber-optic network.

GE Intelligent Platforms ***strongly recommends*** two redundancy links (a total of four RMX modules) be configured and installed. Optionally, systems can be configured for a single redundancy link (a total of two RMX modules).

When the RMX is being used as link in a redundancy system, it cannot be used as a general-purpose Memory Xchange module. For details on the operation of a PACSystems CPU redundancy system, refer to GFK-2308, *PACSystems Hot Standby CPU Redundancy User's Manual*.

A PACSystems RX3i main rack supports a maximum of six Memory Xchange modules in any combination of RMX128, CMX128, and RMX228 modules. A maximum of two RMX modules can be configured as redundancy communication links.

Features

- PACSystems RX3i single slot form factor.
- 128 Mbytes reflective memory. †
- Software configuration of all node parameters (no jumper or switch settings required). †
- High-speed easy-to-use 2.12 Gbaud fiber-optic network.
- No RX3i CPU processing required to operate the network.
- Network-compatible with VMIC 5565 family of reflective memory devices, including the RX7i CMX/RMX module.
- Connection with multimode fiber up to 300 m/984.25 ft.
- Dynamic packet sizes of 4 to 68 bytes, controlled by the RMX128 module when configured to operate as a CMX128 module.
- Programmable module interrupt output.
- Four general-purpose network interrupts with 32 bits of data each. †
- Network error detection.
- Up to 256 nodes per network.†
- Redundant transfer mode operation. This optional mode reduces the chance of a data packet being dropped from the network. †
- Configurable network memory offset allows you to assign nodes on a network to groups according to the 16 MB segment in the network address space that they use. †

The RMX128 module must be located in an RX3i Universal Backplane. The module can be hot-inserted and removed following the instructions in the GFK-2314, *PACSystems RX3i System Manual*.

† Not available when operating as a redundancy link in a CPU redundancy system.

Specifications

Packet size	Dynamic, automatically controlled by RMX128 module
User memory	128 MB SDRAM
Input power (from RX3i power supply)	580 mA @ +3.3VDC 220 mA @ +5VDC
Connectors	■ Fiber-optic LC type, conforms to IEC 61754-20 ■ Zirconium ceramic ferrule ■ Insertion loss: 0.35 dB (maximum) ■ Return loss: -30dB

Refer to the *PACSystems RX3i System Manual (*GFK-2314), for product standards and general specifications.

Related Publications

Available at www.ge-ip.com/support

PACSystems CPU Reference Manual (GFK-2222)
PACSystems RX3i System Manual (GFK-2314)

PACSystems Installation and Maintenance Requirements (GFK-2975) or later
PACSystems Memory Xchange Modules User's Manual (GFK-2300)
PACSystems RX3i Ethernet NIU User's Manual (GFK-2439)
PACSystems Hot Standby CPU Redundancy User's Guide (GFK-2308)

Ordering Information

Description	***Catalog Number***
Reflective Memory Xchange Module for RX3i	IC695RMX128
Multimode Fiber-optic Cables	VMICBL-000-F5-*0xx*, where *0xx* distinguishes different lengths
Reflective Memory Hub	*VMIACC-5595*

Installation and Maintenance

Refer to *PACSystems Installation and Maintenance Requirements* (GFK-2975) to ensure safe use guidelines are followed for each installation environment.

Release History

Release	Firmware Version	Date	Comments
IC695RMX128-FH	HW -Fx 2.01	Mar. 2016	**Hardware change:** Power Cycle issue that in rare cases after cycling power on the module could result in "loss of module" during power up. A subsequent power cycle will clear this condition. Refer to the section Problems Resolved by Hardware version -Fx. **Firmware Version 2.01**In rare cases a timing issue occurs after a power cycle resulting in a "loss of module" during power up. A subsequent power cycle will clear this condition. Refer to the section *Problems Resolved by Firmware Release 2.01*.
IC695RMX128-EG	2.00	Jul. 2015	This change just further enhances the designs' resistance to the rare condition of corruption during a memory read from occurring.
IC695RMX128-DG	2.00	Sep. 2013	Hardware update to resolve a component obsolescence issue. No changes to features, functions or compatibility.
IC695RMX128-CG	2.00	Jul. 2013	This update prevents a rare memory read data corruption issue from occurring.
IC695RMX128-BF	1.07	Feb. 2013	This firmware update enhances the data corruption self-correcting mechanism to provide additional detection and correction capability for memory reads.
IC695RMX128-BE	1.06	Dec. 2012	This hardware update addresses a rare condition in which some units may exhibit an impedance between system 0V and earth ground that is lower than the designed value.
IC695RMX128-AE	1.06	Oct. 2012	The mechanism used to report the memory read data corruption via the parity error LISR bit and interrupt has been removed in version 1.06 in favor of a new self-correcting mechanism that is transparent to the user application and handled internally by the CPU (beginning with CPUv7.17).
IC695RMX128-AC	1.04	Aug. 2011	Increases the maximum packet size that can be accepted and processed to 68 bytes *when configured to operate as a CMX128 module*. Adds the ability to detect and correct a rarely occurring condition of corruption in data read operations.
IC695RMX128-AB	1.01	Feb. 2009	Initial release.

Important Product Information for this Release

Upgrades

Do not install firmware version 2.00 or later on hardware versions –Ax or –Bx. This will render the unit inoperable and will require the unit be returned to the factory.

Do not install firmware versions earlier than 2.00 on hardware versions –Cx or later. This will render the unit inoperable and will require the unit be returned to the factory.

Functional Compatibility

The RMX requires the following versions for configuration and operation.

Subject	*Description*
Programmer Version Requirements	PME version 5.90 SIM1 or later must be used for compatibility with the RMX128 module.
RX3i CPU	RX3i CPU firmware version 7.75 (or later) is required to be used with RMX128 hardware version 2.00 (-Cx) or later and firmware version 2.00 or later. PACSystems RX3i CRU320 is required for use in a redundancy system.
RMX128 Versions	Firmware version 2.00 is not compatible with earlier hardware versions. Firmware versions earlier than 2.00 are not compatible with 2.00 and later (-Cx and later) hardware versions.
Rack Location	The RMX128 must be located in the main RX3i rack. IC695RMX128 modules require a PCI backplane, which is not available on IC694CHSxxx expansion bases.

Problems Resolved by Hardware version -Fx

Subject	*Description*

RMX does not always power up	Power Cycle issue that in rare cases after cycling power on the module could result in “loss of module” during power up. A subsequent power cycle will clear this condition. The fault we have seen when this issue occurs is as follows:
	`Group:4 LOSS_OTHR_MOD - Loss of or missing option module`
	`Error Code:94 Failure during module proxy initialization or startup`
	`Extra Data: 01 72 06 a2 80 08 0a 04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00`

Problems Resolved by Firmware Release 2.01

Subject	*Description*

RMX does not always power up	Power Cycle issue that in rare cases after cycling power on the module could result in “loss of module” during power up. A subsequent power cycle will clear this condition. The fault we have seen when this issue occurs is as follows:
	`Group:4 LOSS_OTHR_MOD - Loss of or missing option module`
	`Error Code:94 Failure during module proxy initialization or startup`
	`Extra Data: 01 72 06 a2 80 12 18 2d 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00`
	
	This issue has been fixed in RMX firmware version 2.01 and later.
	Firmware version 2.01 is available to download in an upgrade kit.
	IMPORTANT: Firmware version 2.01 can only be used on Hardware versions –Cx and later.

Restrictions and Open Issues in this Release

Subject	Description
RX3i RMX/CMX modules require grounded ESD strap for EMC Installation	When installing, operating, or maintaining the IC695RMX128, personnel must ensure any electrostatic charge is discharged through the use of a grounded ESD strap or other means to meet IEC-61000-4-2 (ESD) requirements. A direct electrostatic discharge event of 4kV or higher applied to the metal optical transceiver housing may result in a lights out module requiring a power cycle to recover.
RX3i RMX and CMX modules require a metal enclosure to meet radiated emissions requirements.	For installation requirements, refer to the *EMC Installation Requirements* section on page **Error! Bookmark not defined.**.
RX3i CMX/RMX does not disable transmitter when the CPU goes to Stop/Halt mode.	For IC695CMX128 and IC695RMX128 modules not used as redundancy links, the automatic transmitter disable feature currently does not work correctly when a controller goes to Stop/Halt mode. When the CPU goes to Stop/Halt mode or fails and the automatic transmitter disable feature is enabled, the fiber-optic transmitter should be turned off, breaking the reflective memory link. When the feature is disabled, the transmitter remains ON and the reflective memory link will not be broken. If this feature is enabled, the automatic transmitter disable feature does not work when the CPU goes into Stop/Halt mode (such as after a software watchdog trip or multi-bit ECC error detection) leaving the fiber-optic transmitter ON. The fiber-optic transmitter is properly disabled if the CPU fails or is lost (for instance the CPU hardware is removed, the CPU experiences a hardware watchdog event, or displays a blink code such as a page fault). This user-configurable feature is enabled by default. The feature may be disabled by clearing bit 12 with a BUS_WRITE to region 3, offset 0x440.
Parity error received after extended run on RMX module.	Infrequently, if parity is enabled on the RMX128 module when it is not used as a Redundancy link, the module may intermittently report a false parity error, although the associated data is valid. The problem is more likely to occur when the same memory locations are simultaneously and constantly accessed from both the network and the RX3i backplane side.
The LCSR status bit is not turning ON after LISR turns ON when Interrupt (Sync Loss) is generated.	When a sync loss condition is detected the LISR bit is latched ON but the LCSR sync loss bit is not latched ON (that is, it remains OFF). To check the sync loss status, monitor the sync loss bit in the LISR register instead of the LCSR sync loss bit.
SVC_REQ 17 is not supported	SVC_REQ 17 is not supported to mask or unmask module interrupts on RX3i CPUs. There is currently no way to identify which module interrupt should be masked on RX3i. For RX7i this was handled by a table of values, but this table of values is invalid on RX3i. Instead the customer should simply turn off interrupts using the normal interrupt disabling mechanism as described in the user's manual.

Operational Notes

Bad Data Interrupt	To prevent continuous interrupts when the Bad Data Interrupt is enabled, you may want to temporarily set bit 8 in the LIER to 0 when a sync loss condition is detected. If your application is also using the Sync Loss Interrupt, you may also want to temporarily set bit 11 in the LIER to zero when the sync loss condition is detected. You can then re-enable the Bad Data Interrupt (and Sync Loss Interrupt if it was also disabled) when the sync loss condition has been corrected.